WE CLAIM:

1. A spread-spectrum-matched filter, for use as part of a spread-spectrum receiver on a received-spread-spectrum signal having a plurality of information bits, with the received-spread-spectrum signal generated from spread-spectrum processing each information bit with a chip-sequence signal, comprising:

a first plurality of shift registers for storing a first portion of a reference-chip-sequence signal;

a second plurality of shift registers for storing a second portion of the reference-chip-sequence signal;

a control processor for generating a clock signal having a clock rate with a clock cycle;

a multiplexer, coupled to said first plurality of shift registers and to said second plurality of shift registers, responsive to the clock signal, for outputting, from said first plurality of shift registers through said multiplexer, the first portion of the reference-chip-sequence signal during a first portion of the clock cycle, and for outputting, from said second plurality of shift registers through said multiplexer, the second portion of the reference-chip-sequence signal during a second portion of the clock cycle;

a plurality of data-shift registers, coupled to said spread-spectrum receiver, for shifting a plurality of input-data samples of the received-spread-spectrum signal at the clock rate;

a plurality of exclusive-OR (XOR) gates, coupled to said plurality of data-shift registers and through said

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multiplexer to said first plurality of shift registers and through said multiplexer to said second plurality of shift registers, responsive to said multiplexer selecting the first plurality of shift registers during the first portion of the clock cycle, for multiplying the first portion of the reference-chip-sequence signal by the plurality of input-data samples during the first portion of the clock cycle, thereby outputting a first plurality of product-output signals, and responsive to said multiplexer selecting the second plurality of shift registers during the second portion of the clock cycle, for multiplying the second portion of the reference-chip-sequence signal by the plurality of input-data samples during the second portion of the clock cycle, thereby outputting a second plurality of product-output signals;

an adder tree, comprising a plurality of adder gates coupled to said plurality of XOR gates, for summing the first plurality of product-output signals during the first portion of the clock cycle, thereby generating a first sum, and for summing the second plurality of product-output signals during the second portion of the clock cycle thereby generating a second sum;

a memory, coupled to said adder tree, for storing the first sum outputted from said adder tree during the first portion of the clock cycle; and

an adder, coupled to said adder tree and to said memory, for adding the first sum stored in said memory to the second sum from said adder tree.

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2. The spread-spectrum-matched filter as set forth in claim 1, further comprising an AND gate coupled to said control processor for inhibiting the clock signal to said first plurality of shift registers and to said second plurality of shift registers.

3. The spread-spectrum-matched filter as set forth in claim 1, further comprising an AND gate coupled to an input of each shift register of said first plurality of shift registers for inhibiting operation of said first plurality of shift registers.

4. The spread-spectrum-matched filter as set forth in claim 1, further comprising an AND gate coupled to an input of each shift register of said second plurality of shift registers for inhibiting operation of said second plurality of shift registers.

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5. A spread-spectrum-matched filter, for use as part of a spread-spectrum receiver on a received-spread-spectrum signal having a plurality of information bits with the received-spread-spectrum signal generated from spread-spectrum processing each information bit with a chip-sequence signal, comprising:

reference means for storing a plurality of portions of a reference-chip-sequence signal;

control means for generating a clock signal having a clock rate with a clock cycle;

multiplexer means, coupled to said reference means and responsive to the clock signal, for outputting, sequentially, from said reference means and through said multiplexer means, each portion of the plurality of portions of the reference-chip-sequence signal during a respective portion of the clock cycle;

data means, coupled to said spread-spectrum receiver, for shifting a plurality of input-data samples of the received-spread-spectrum signal at the clock rate;

multiplying means, coupled to said data means and through said multiplexer means to said reference means, responsive to said multiplexer means selecting during each portion of the clock cycle, for multiplying the respective portion of the reference-chip-sequence signal by the plurality of input-data samples located in said data means during the respective portion of the clock cycle, thereby outputting a respective plurality of product-output signals;

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summing means, coupled to said multiplying means, for summing each plurality of product-output signals during the respective portion of the clock cycle, thereby generating a plurality of sums corresponding to the plurality of portions of the reference-chip-sequence signal;

memory means, coupled to said summing means, for storing at least N-1 sums of the plurality of N sums; and

adder means, coupled to said summing means and to said memory means, for adding the plurality of sums.

6. The spread-spectrum-matched filter as set forth in claim 5, further comprising an AND gate coupled to said control means for inhibiting the clock signal to said reference means.

7. The spread-spectrum-matched filter as set forth in claim 5, further comprising an AND gate coupled to said reference means for inhibiting operation of said first plurality of shift registers.

8. The spread-spectrum-matched filter as set forth in claim 5, with said reference mean including:

a first plurality of shift registers for storing a first portion of a reference-chip-sequence signal; and

a second plurality of shift registers for storing a second portion of the reference-chip-sequence signal.

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9. The spread-spectrum-matched filter as set forth in claim 8 with said multiplexer means including a multiplexer coupled to said first plurality of shift registers and to said second plurality of shift registers, responsive to the clock signal, for outputting, from said first plurality of shift registers and through said multiplexer, the first portion of the reference-chip-sequence signal during a first portion of the clock cycle, and for outputting, from said second plurality of shift registers and through said multiplexer, the second portion of the reference-chip-sequence signal during a second portion of the clock cycle.

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10. The spread-spectrum-matched filter as set forth in claim 9, with said multiplying means including a plurality of exclusive-OR (XOR) gates, coupled to said data means and through said multiplexer to said first plurality of shift registers and through said multiplexer to said second plurality of shift registers, responsive to the multiplexer selecting the first plurality of shift registers during the first portion of the clock cycle, for multiplying the first portion of the reference-chip-sequence signal by the plurality of input-data samples during the first portion of the clock cycle, thereby outputting a first plurality of product-output signals, and responsive to said multiplexer selecting the second plurality of shift registers during the second portion of the clock cycle, for multiplying the second portion of the reference-chip-sequence signal by the plurality of input-data samples during the second portion of the clock cycle, thereby outputting a second plurality of product-output signals.

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11. A spread-spectrum-matched filter, for use as part of a spread-spectrum receiver on a received-spread-spectrum signal having a plurality of information bits with the received-spread-spectrum signal generated from spread-spectrum processing each information bit with a chip-sequence signal, comprising:

first reference means for storing a first portion of a reference-chip-sequence signal;

second reference means for storing a second portion of the reference-chip-sequence signal;

control means for generating a clock signal having a clock rate with a clock cycle;

multiplexer means, coupled to said first reference means and to said second reference means and responsive to the clock signal, for outputting, from said first reference means, through said multiplexer means, the first portion of the reference-chip-sequence signal during a first portion of the clock cycle, and for outputting, from said second reference means, the second portion of the reference-chip-sequence signal during a second portion of the clock cycle;

data means, coupled to said spread-spectrum receiver, for shifting a plurality of input-data samples of the received-spread-spectrum signal at the clock rate;

multiplying means, coupled to said data means and through said multiplexer means to said first reference means and through said multiplexer means to said second reference means, responsive to said multiplexer means selecting the first reference means during the first portion of the clock cycle, for

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multiplying the first portion of the reference-chip-sequence signal by the plurality of input-data samples located in said data means during the first portion of the clock cycle, thereby outputting a first plurality of product-output signals, and responsive to said multiplexer means selecting the second reference means during the second portion of the clock cycle, for multiplying the second portion of the reference-chip-sequence signal by the plurality of input-data samples located in said data means during the second portion of the clock cycle, thereby outputting a second plurality of product-output signals;

adder-tree means coupled to said multiplying means, for summing the first plurality of product-output signals during the first portion of the clock cycle, thereby generating a first sum, and for summing the second plurality of product-output signals during the second portion of the clock cycle thereby generating a second sum;

memory means, coupled to said adder-tree means, for storing the first sum; and

adder means, coupled to said adder-tree means and to said memory means, for adding the first sum stored in said memory means to the second sum from said adder tree.

12. The spread-spectrum-matched filter as set forth in claim 11, further comprising an AND gate coupled to said control means for inhibiting the clock signal to said first reference means and to said second reference means.

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13. The spread-spectrum-matched filter as set forth in claim 8, further comprising an AND gate coupled to an input of each shift register of said first plurality of shift registers for inhibiting operation of said first plurality of shift registers.

14. The spread-spectrum-matched filter as set forth in claim 8, further comprising an AND gate coupled to an input of each shift register of said second plurality of shift registers for inhibiting operation of said second plurality of shift registers.

15. The spread-spectrum-matched filter as set forth in claim 11, with said reference means including:

a first plurality of shift registers for storing a first portion of a reference-chip-sequence signal; and

a second plurality of shift registers for storing a second portion of the reference-chip-sequence signal.

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16. The spread-spectrum-matched filter as set forth in claim 15 with said multiplexer means including a multiplexer coupled to said first plurality of shift registers and to said second plurality of shift registers, responsive to the clock signal, for outputting, from said first plurality of shift registers, through said multiplexer, the first portion of the reference-chip-sequence signal during a first portion of the clock cycle, and for outputting, from said second plurality of shift registers, through said multiplexer, the second portion of the reference-chip-sequence signal during a second portion of the clock cycle.

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17. The spread-spectrum-matched filter as set forth in claim 16, with said multiplying means including a plurality of exclusive-OR (XOR) gates, coupled to said data means and through said multiplexer to said first plurality of shift registers and through said multiplexer to said second plurality of shift registers, responsive to the multiplexer selecting the first plurality of shift registers during the first portion of the clock cycle, for multiplying the first portion of the reference-chip-sequence signal by the plurality of input-data samples during the first portion of the clock cycle, thereby outputting a first plurality of product-output signals, and responsive to said multiplexer selecting the second plurality of shift registers during the second portion of the clock cycle, for multiplying the second portion of the reference-chip-sequence signal by the plurality of input-data samples during the second portion of the clock cycle, thereby outputting a second plurality of product-output signals.

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